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EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 01/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/621,908	**Applicant(s)** DHONG ET AL.	
	Examiner Benjamin P. Geib	**Art Unit** 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003 and 02 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 28-31* is/are rejected.

7)☒ Claim(s) *26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-31 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 07/17/2003 and Power of Attorney on 09/02/2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 5-6, and 29-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Chehrazi et al., U.S. Patent No. 6,282,556 (Herein referred to as Chehrazi).

5. Referring to claim 1, Chehrazi has taught a byte execution unit, comprising: logic coupled to receive byte instruction information and two operands and configured to perform an operation specified by the byte instruction information upon at least one of the two operands, thereby producing a result *(column 7, lines 21-51)*, wherein the byte instruction specifies either a count ones in bytes operation, an average bytes operation *(See Table I, instruction AVG)*, an absolute differences of bytes operation *(column 3, lines 49-54)*, or a sum bytes into halfwords operation.

6. Referring to claim 2, Chehrazi has taught the byte execution unit as recited in claim 1, wherein each of the two operands comprises a plurality of bits, and wherein the bits of the two operands are grouped to form a plurality of corresponding 8-bit bytes *(column 7, lines 23-27; See Fig. 2, component 210).*

7. Referring to claim 3, Chehrazi has taught the byte execution unit as recited in claim 2, wherein each of the two operands comprises 128 bits, and wherein the bits of the two operands are grouped to form 16 corresponding bytes *(column 7, lines 23-27; See Fig. 2, component 210).*

8. Referring to claim 5, Chehrazi has taught the byte execution unit as recited in claim 2, wherein in the event the byte instruction information specifies the average bytes operation, the byte execution unit is configured to compute averages of corresponding bytes of the two operands, and wherein the result is indicative of the averages *(column 13, lines 12-20).*

9. Referring to claim 6, Chehrazi has taught the byte execution unit as recited in claim 2, wherein in the event the byte instruction information specifies the absolute differences of bytes operation, the byte execution unit is configured to subtract a value of a byte of one of the two operands from a value of a corresponding byte of the other operand, and to compute an absolute value of a result of the subtraction operation, and wherein the result is indicative of the absolute value of the result of the subtraction operation *(column 3, lines 49-54, column 9, lines 6-15).*

10. Referring to claim 29, Chehrazi has taught a data processing system, comprising:

a memory system *(Fig. 1, component 102; column 5, lines 46-54)* comprising a byte instruction, wherein the byte instruction specifies either a count ones in bytes operation, an average bytes operation *(See Table I, instruction AVG)*, an absolute differences of bytes operation *(column 3, lines 49-54)*, or a sum bytes into halfwords operation; and

a processor *(multimedia coprocessor; Fig. 1, component 108)* coupled to the memory system and configured to fetch and execute instructions from the memory system *(column 7, lines 21-40)*, wherein the processor comprises:

> a byte execution unit coupled to receive byte instruction information and two operands and configured to perform an operation specified by the byte instruction information upon at least one of the two operands, thereby producing a result *(column 7, lines 21-51)*.

11. Referring to claim 30, given the similarities between claim 2 and claim 30 the arguments as stated for the rejection of claim 2 also apply to claim 30.

12. Referring to claim 31, given the similarities between claim 3 and claim 31 the arguments as stated for the rejection of claim 3 also apply to claim 31.

13. Claims 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Peleg et al., U.S. Patent No. 6,070,237 (Herein referred to as Peleg).

14. Referring to claim 15, Peleg has taught a logic system, comprising:

compressor logic *(4-to-2 CSA; Fig. 10, component 1030)* coupled to receive an 4n-bit operand *[12-bit operand (i.e. n = 3)]* and configured to perform a compression operation upon the operand *(The operand is compressed from 12-bits to 8-bits; See Fig. 10)*, thereby producing a plurality of compressor output signals *(column 14, 52-65)*; and

adder logic *(FA; Fig. 10, component 1050)* coupled to receive the compressor output signals and configured to perform an addition operation upon the compressor output signals, thereby producing an (n+2)-bit *(5-bit)* result *(See Fig. 10; column 14, 52-65)*.

15. Referring to claim 16, Peleg has taught the logic system as recited in claim 15, wherein the addition operation comprises an (n+1)-bit *(4-bit)* addition operation *(See Fig. 10; column 14, lines 64-65)*.

16. Referring to claim 17, Peleg has taught the logic system as recited in claim 16, wherein the adder logic comprises an n-bit adder *(The 4-bit adder can add inputs with sizes up to 4-bit. Since that range includes 3-bit inputs, the adder is a 3-bit adder)*.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 4, 19-24, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi in view of Peleg.

19. Referring to claim 4, Chehrazi has taught the byte execution unit as recited in claim 2.

Chehrazi has not taught that the byte instruction information can specify a count ones in bytes operation and, in the event the byte instruction information specifies the count ones in bytes operation, the byte execution unit is configured to count a number of logic one bits in each of the bytes of one of the two operands, and wherein the result is indicative of the number of logic one bits in each of the bytes.

Peleg has taught that byte instruction information can specify a count ones in bytes operation *(Peleg; population count operation)* and in the event the byte instruction information specifies the count ones in bytes operation, the byte execution unit is configured to count a number of logic one bits in each of the bytes of one of the two operands, and wherein the result is indicative of the number of logic one bits in each of the bytes *(Peleg; column 10, line 47 – column 11, line 17)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Chehrazi to include the count ones in bytes operation as taught by Peleg.

The suggestion/motivation for doing so would have been that Peleg has taught doing so improves the performance of algorithms requiring the totaling of the number of bits set *(Peleg; column 4, lines 13-16)*.

20. Referring to claim 19, Chehrazi has taught a byte execution unit, comprising:

a plurality of byte units, wherein each byte unit comprises:

a first compressor unit *(Fig. 5a, component 326a)* coupled to receive a portion of the first operand and configured to produce a first plurality of compressor output signals dependent upon the first operand *(column 7, line 56 – column 8, line 9; column 10, lines 2-6)*;

a second compressor unit *(Fig. 5b, component 326b)* coupled to receive a portion of the second operand and configured to produce a second plurality of compressor output signals dependent upon the second operand *(column 7, line 56 – column 8, line 9; column 10, lines 27-31)*;

adder input multiplexer logic *(Fig. 5a, component 332a & Fig. 5b, component 332b)* coupled to receive the first and second pluralities of compressor output signals as data input signals *(column 8, lines 10-16)*, and a first plurality of control signals, and configured to produce a portion of the data input signals as output signals dependent upon the first plurality of control signals;

adder logic *(Fig. 5a, component 340a & Fig. 5b, component 340b)* coupled to receive the output signals produced by the adder input multiplexer logic and configured to produce a plurality of adder output signals dependent upon the output signals produced by the adder input multiplexer logic *(column 10, lines 6-9, 31-34)*; and

wherein the byte execution unit is coupled to receive byte instruction information *(column 7, lines 21-36)*, and wherein the first and second pluralities of control signals are indicative of the byte instruction information *(See Fig. 4,* *control signals indicating particular types of instructions)*, and wherein the byte instruction information specifies either a count ones in bytes operation, an average bytes operation *(See Table I, instruction AVG)*, an absolute differences of bytes operation *(column 3, lines 49-54)*, or a sum bytes into halfwords operation.

Chehrazi has not taught a plurality of population counters each coupled to receive a portion of a first operand and configured to produce a population output signal indicative of a number of logic ones in the corresponding portion of the first operand and, further, that the output signal is received by the adder input multiplexer.

Peleg has taught a plurality of population counters *(POPCNT Circuits; Fig. 9, components 908a-d)* each coupled to receive a portion of a first operand and configured to produce a population output signal indicative of a number of logic ones in the corresponding portion of the first operand *(Peleg; column 14, line 5-36)*. Peleg has also taught that the output signal of the plurality of population counters requires further addition (See additional adders in Fig. 9).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Chehrazi to include a plurality of population counters as taught by Peleg since Peleg has taught doing so improves the performance of algorithms requiring the totaling of the number of bits set *(Peleg; column 4, lines 13-16)*. It further would have been obvious to a person of ordinary skill in the art at the time the invention was made to receive the output signal by an adder input multiplexer since the output signal requires further addition and one of ordinary skill in the art would have recognized that sharing the adder through the use of a multiplexer would beneficially reduce the amount of hardware needed in the byte execution unit.

Chehrazi does not disclose expressly result multiplexer logic coupled to receive the adder output signals as data input signals, and a second plurality of control signals, and configured to produce a portion of the data input signals as a result signal dependent upon the second plurality of control signals .

Peleg discloses result multiplexer logic coupled to receive data input signals, and a plurality of control signals, and configured to produce a portion of the data input signals as a result signal dependent upon the plurality of control signals *(column 15, lines 31-35)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify Chehrazi to include the result multiplexer logic as taught by Peleg.

The suggestion/motivation for doing so would have been that multiple circuits are allowed to write onto the result bus *(Peleg; column 15, lines 31-35)*.

21. Referring to claim 20, Chehrazi and Peleg have taught the byte execution unit as recited in claim 19, wherein the first and second operands each comprise a plurality of bits, and wherein the bits of the first and second operands are grouped to form a plurality of corresponding 8-bit bytes *(Chehrazi; column 7, lines 23-27; See Fig. 2, component 210)*.

22. Referring to claim 21, Chehrazi and Peleg have taught the byte execution unit as recited in claim 20, wherein the first and second operands each comprise 128 bits, and wherein the bits of the first and second operands are grouped to form 16 corresponding bytes *(Chehrazi; column 7, lines 23-27; See Fig. 2, component 210).*

23. Referring to claim 22, Chehrazi and Peleg have taught the byte execution unit as recited in claim 20, wherein in the event the byte instruction information specifies the count ones in bytes operation, the result signal is indicative of a number of logic one bits in each of the bytes of the first operand *(Peleg; column 10, line 47 – column 11, line 17).*

24. Referring to claim 23, Chehrazi and Peleg have taught the byte execution unit as recited in claim 20, wherein in the event the byte instruction information specifies the average bytes operation, the result signal is indicative of averages of corresponding bytes of the first and second operands *(Chehrazi; column 13, lines 12-20).*

25. Referring to claim 24, Chehrazi and Peleg have taught the byte execution unit as recited in claim 20, wherein in the event the byte instruction information specifies the absolute differences of bytes operation, the result signal is indicative of an absolute value of a result of subtraction operations wherein bytes of the first operand are subtracted from the corresponding bytes of the second operand *(Chehrazi; column 3, lines 49-54, column 9, lines 6-15).*

26. Referring to claim 28, Chehrazi and Peleg have taught the byte execution unit as recited in claim 20, wherein the adder logic comprises a plurality of 8-bit compound adders *(The adder logic comprises 4 adders, each of which is capable of adding 8 bits*

and is therefore an 8-bit adder. These adders are compounded together to form a larger adder and therefore are compound adders – column 8, lines 23-26).

27. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi in view of Oberman et al., "AMD 3DNow! Technology: Architecture and Implementations" (Herein referred to as Oberman).

28. Referring to claim 7, Chehrazi has taught the byte execution unit as recited in claim 2.

Chehrazi has not taught that the byte instruction information can specify the sum bytes into halfwords operation and, in the event the byte instruction information specifies the sum bytes into halfwords operation, the byte execution unit is configured to compute sums of values of a number of consecutive bytes of the two operands, and wherein the result is indicative of the sums.

Oberman has taught that byte instruction information can specify a sum bytes into halfwords operation *(Oberman; PFACC instruction)* and in the event the byte instruction information specifies the sum bytes into halfwords operation, the byte execution unit is configured to compute sums of values of a number of consecutive bytes of the two operands, and wherein the result is indicative of the sums *(Oberman; see "Basic arithmetic instructions" section on page 39).*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Chehrazi to include the sum bytes into halfwords operation as taught by Oberman.

29. The suggestion/motivation for doing so would have been that Oberman has taught doing enables "full utilization of computing resources when performing dot-product-style summations" *(Oberman; see "Basic arithmetic instructions" section on page 39)*.

30. Claims 8-10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oberman.

31. Referring to claim 8, Oberman has taught a byte execution unit, comprising:

pre-processing logic *(logic from "data format selection" unit to multiplexer unit; Fig. 4)* coupled to receive a plurality of operands and configured to perform an operation upon the operands dependent upon an operation specified by a byte instruction, thereby producing an intermediate result *(Multiplier Section; Page 43-44)*;

adder logic *(carry-propagate adder; Fig.4)* coupled to receive the intermediate result and configured to perform an addition operation upon the intermediate result, thereby producing a sum *(Multiplier Section; Page 43-44)*; and

post-processing logic *(final result selection logic; Fig. 4)* coupled to receive the sum and configured to perform an operation *(a selection operation)* upon the sum dependent upon the operation specified by a byte instruction *(The control signal* *indicating overflow, which is dependent upon the operation specified by a instruction, selects the result)*, thereby producing a result *(Multiplier Section; Page 43-44)*.

Oberman has not explicitly taught that the adder logic produces a sum+1 and that the post-processing logic receives the sum+1 and performs an operation on it.

Oberman teaches adder logic *(compound adder)* that produces a sum+1 output and post-processing logic *(selection logic)* that receives the sum+1 and performs an operation on it *(Last paragraph in first column on page 43)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the adder logic and post-processing logic of Oberman to produce a sum+1 and receive the sum+1 and perform an operation on it, respectively, as taught by Oberman.

The suggestion/motivation for doing so would have been that the time required for rounding is reduced *(Last paragraph in first column on page 43)*.

32. Referring to claim 9, Oberman has taught the byte execution unit as recited in claim 8, wherein the byte instruction specifies either a count ones in bytes operation, an average bytes operation, an absolute differences of bytes operation, or a sum bytes into halfwords operation *(PFACC instruction; see "Basic arithmetic instructions" section on page 39)*.

33. Referring to claim 10, Oberman has taught the byte execution unit as recited in claim 8.

Oberman has not explicitly taught that the pre-processing logic and the post-processing logic are each coupled to receive control signals indicative of the operation specified by the byte instruction.

However, Examiner takes Official Notice that processing logic coupled to receive control signals indicative of the operation specified by the instruction being processed is conventional and well-known in order to control the operation of the processing logic.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the pre-processing and post-processing logic of Oberman to receive control signals indicative of the operation specified by the bytes instruction since Examiner takes Official Notice that processing logic coupled to receive control signals indicative of the operation specified by the instruction being processed is conventional and well-known in order to control the operation of the processing logic.

34. Referring to claim 12, Oberman has taught the byte execution unit as recited in claim 8, wherein the pre-processing logic comprises compressor logic *(See Fig. 4, 4:2 compressor)* coupled to receive the operands and configured to perform a compression function *(Multiplier Section; Page 43-44)*.

35. Referring to claim 13, Oberman has taught the byte execution unit as recited in claim 8, wherein the post-processing logic comprises end-around carry logic *(selection logic)* configured to perform an end-around carry function *(selection function) (The carry from the end of the addition operation and is routed around to the selection mechanism to select the appropriate result - See first paragraph in the first column on page 44)*.

36. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oberman in view of "IA-64 Application Developer's Architecture Guide" (Herein referred to as Guide).

37. Referring to claim 14, Oberman has taught the byte execution unit as recited in claim 8 wherein the byte instruction specifies an average operation *(Oberman; See Table 1, PAVGUSB instruction).*

Oberman has not explicitly taught that the post-processing logic is configured to perform bit shift operations.

Guide has taught post-processing logic that performs bit shift operations *[After the addition of the elements is performed (i.e. post-processing) the output is shifted (Guide; "Parallel Average" instruction description on page 7-140 and Fig. 7-29 on page 7-141].*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the post-processing of Oberman to perform bit shift operations as taught by Guide.

The suggestion/motivation for doing so would have been that performing bit shift operations in post-processing logic allows an average instruction, like that taught by Oberman, to execute an averaging operation while preventing cumulative round-off errors (*Guide; "Parallel Average" instruction description on page 7-140*) and without a time-consuming division operation *(Guide; See Fig. 7-29 on page 7-141).*

38. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oberman in view of Peleg.

39. Referring to claim 11, Oberman has taught the byte execution unit as recited in claim 8.

Oberman has not taught that the pre-processing logic comprises population counter logic coupled to receive the operands and configured to produce population output signals indicative of numbers of logic ones in portions of the operands.

Peleg has taught pre-processing logic that comprises a population counter logic *(POPCNT Circuits; Fig. 9, components 908a-d)* coupled to receive the operands and configured to produce population output signals indicative of numbers of logic ones in portions of the operands *(Peleg; column 14, line 5-36)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the pre-processing logic of Oberman to include the population counter logic as taught by Peleg.

The suggestion/motivation for doing so would have been that Peleg has taught doing so improves the performance of algorithms requiring the totaling of the number of bits set *(Peleg; column 4, lines 13-16)*.

40. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peleg.

41. Referring to claim 18, Peleg discloses the logic system as recited in claim 17.

Peleg does not expressly disclose that n=8 *(i.e. the input operand is 32-bit).*

However, Examiner takes Official Notice that extending the size of compressor and adder logic to accommodate a 32-bit input operand is conventional and well known in order to process more data at once.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the compressor and adder logic system as taught by Peleg to accommodate a 32-bit input operand since Examiner takes Official Notice that extending the size of compressor and adder logic to accommodate a 32-bit input operand is a conventional and well known in order to process more data at once.

42. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chehrazi in view of Peleg, as applied to claims 19-20 above, and further in view of Oberman.

43. Referring to claim 25, Chehrazi and Peleg have taught the byte execution unit as recited in claim 20.

Chehrazi and Peleg have not taught that the byte instruction information can specify the sum bytes into halfwords operation and, in the event the byte instruction information specifies the sum bytes into halfwords operation, the result signal is indicative of sums of values of consecutive bytes of the first and second operands.

Oberman has taught that byte instruction information can specify a sum bytes into halfwords operation *(Oberman; PFACC instruction)* and in the event the byte instruction information specifies the sum bytes into halfwords operation, the result is indicative of sums of values of consecutive bytes of the first and second operands *(Oberman; see "Basic arithmetic instructions" section on page 39).*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Chehrazi and Peleg to include the sum bytes into halfwords operation as taught by Oberman.

The suggestion/motivation for doing so would have been that Oberman has taught doing enables "full utilization of computing resources when performing dot-product-style summations" *(Oberman; see "Basic arithmetic instructions" section on page 39).*

Allowable Subject Matter

44. Claims 26 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

45. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

46. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abdallah et al., U.S. Patent No. 6,243,803, teaches a byte processor that executes an absolute differences operation on byte data.

Johnson et al., U.S. Patent Publication No. 2004/0199751, teaches a byte processor that executes a sum of absolute differences operation on byte data.

Tyler et al., "AltiVec: Bringing Vector Technology to the PowerPC Processor Family", teaches a byte processor that executes instructions on packed byte data.

Mittal et al., "MMX Technology Architecture Overview", teaches a byte processor that executes instructions on packed byte data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

Henry Tsai 1/17/06

HENRY W. H. TSAI
PRIMARY EXAMINER